REMARKS

Claims 10, 12, 15, 16, 18, 28, and 30 remain in this application. Claims 1-9, 11, 13, 14, 17, 19-27, 29, and 31-38 have been cancelled. Claims 10 and 28 have been amended.

Applicants thank the Examiner for the detailed study of the application and prior art. Applicants have amended independent claims 10 and 28 to place this case in condition for allowance. Applicants also file a Request for Continued Examination with this After Final Amendment.

Independent claim 38 is cancelled.

Dependent claims 13, 14 and 17 have been cancelled.

Claim 10 as amended now recites the plurality of decoupling capacitor assemblies mounted on the integrated circuit die. This integrated circuit die is mounted on the substrate. An example of the integrated circuit die with a plurality of decoupling capacitor assemblies is shown in FIG. 2 in which eight decoupling capacitor subassemblies 38 are physically placed onto center portions of the semiconductor die, using for example, pick and place machinery. Each decoupling capacitor assembly as shown in FIG. 4A includes a capacitor carrier secured onto the exposed surface of the integrated circuit die. A thin film metallization layer is formed on the capacitor carrier. A decoupling capacitor is secured onto this thin film metallization layer. A conductive adhesive layer is positioned between the decoupling capacitor and the thin film metallization layer and secures the decoupling capacitor onto the thin film metallization layer. A wire bond extends from the thin film metallization layer to a logic pin of the integrated circuit die. Another wire bond extends from a logic pin to a substrate bonding pad.

The Examiner argues that the claims are anticipated by U.S. Patent No. 6,005,778 to Spielberger et al. (hereinafter "Spielberger"), or unpatentable over Spielberger in view of U.S. Patent No. 5,140,496 to Heinks et al. (hereinafter "Heinks").

Applicants note that Spielberger is specifically directed to a chip stacking arrangement. Two separate chips have a spacer positioned between the chips. As to the thin metal layer referred to by the Examiner, it is indicated as metal layer 86, shown in FIG. 7. This metal layer 86 is far different from the thin film metallization layer formed on the capacitor carrier. As shown in FIG. 7 of Spielberger, this metal layer extends over the entire chip, as compared to the metal layer in the decoupling capacitor assembly presented in this After Final Amendment, in which the thin film metallization layer is formed on the capacitor carrier with each capacitor carrier having a separate metallization layer. The structure and function of the layer in Spielberger is described in column 4, starting at line 57 and extending through column 5, ending at line 17 as follows:

> "An alternative embodiment which includes a capacitor mounting feature is shown in FIGS. 6 and 7 where discrete capacitors 70 having a conductive end 72 for connection to ground and conductive end 74 for connection to power. For example, type 1206 capacitors may be used. In this embodiment the assembly process is the same as FIG. 5 up through the mounting and connection of second chip 40c. Conductive spacer 80 is a modification of conductive spacer 50 that is described as follows. Conductive surface 82 corresponds to conductive surface 55 of spacer 50. A dielectric material layer 84 such as a

> polymer film or a thick dielectric paste, must be bonded to or deposited on surface 82. Thin metal layer or film 86 is then deposited on top of dielectric layer 84. Openings 88 are then made in metal layer 86 and dielectric layer 84 to expose conductive surface 82 of spacer 80. Capacitors 70 are bonded to spacer 80 with an electrically conductive material 90 such as conductive adhesive or solder or other conductive material. Capacitors 70 then have ends 72 connected to conductive surface 82 and ends 74 connected to metal layer 86. Wire bonds 90 are made between conductive surface 82 and a ground pad on chip 40c or alternatively to a ground pad on package 14c. Additional wire bonds 94 are made from metal layer 86 to a power pad on chip 40c or alternatively to a power pad on package 14c. FIGS. 6 and 7 show the use of a two tiered conductive spacer 40c. However, a spacer having a planar conductive surface could also be used if a portion of the conductive surface were left exposed for connection to ground."

As indicated in the quote above, the thin metal layer (or film) 86 is deposited on the dielectric layer 84. Openings 88 are made in this metal layer 86 to expose the conductive surface 82 of the spacer 80. This structure is far different from the claimed invention as set forth in this After Final Amendment. The metal layer in Spielberger has a different structure and function than the thin film metallization layer formed on the capacitor carrier in the present claimed invention. There is no requirement for openings to be made in the metal layer or any other type of layer in the claimed invention presented in this After Final Amendment, as compared to the structure of Spielberger.

Heinks at most discloses some type of wire bonding used in a decoupling apparatus such as a capacitor, but nowhere suggests the structure and function of the claimed invention as presented in this After Final Amendment.

Accordingly, Applicants contend that the present case is in condition for allowance.

Also, this After Final Amendment also presents the claims in a more readable format, such as stating that the thin film metallization layer is "formed" on the capacitor carrier and the conductive adhesive layer is positioned between the decoupling capacitor and thin film metallization layer. Also, language has been amended to state that the decoupling capacitor is secured onto the thin film metallization layer.

Applicants contend that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due.

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **MAIL STOP AF, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450,** on this 29th day of March, 2006.

Julie Lalan